Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**8 7 6**

**13 14 1**

**9**

**10**

**11**

**12**

**5**

**4**

**3**

**2**

**DIE ID**

**05A**

**.049”**

**.049”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .049” X .049” DATE: 8/18/17**

**MFG: TEXAS INSTRUMENTS THICKNESS .009” P/N: 5405**

**DG 10.1.2**

#### Rev B, 7/19/02